Amendments to the Claims:

1. (Canceled)
2. (Canceled)
3. (Canceled)
4. (Canceled)
5. (Canceled)
6. (Canceled)
7. (Canceled)
8. (Canceled)
9. (Canceled)
10. (Canceled)
11. (Canceled)
12. (New) A method of fabricating a semiconductor package, comprising the steps of:

a) providing a leadframe which includes:

a die paddle having opposed, generally planar top and bottom surfaces; and

a plurality of leads which extend at least partially about the die paddle and each have opposed, generally planar upper and lower lead surfaces and an inner lead end;

b) etching the leadframe such that each of the leads includes a half etched portion which is formed in the lower lead surface, extends to the inner lead end, and defines a generally planar etched lead surface which is disposed in opposed relation to the upper lead surface and extends in generally co-planar relation to the top surface of the die paddle;

c) attaching a semiconductor chip to the top surface of the die paddle;

d) electrically connecting the semiconductor chip to at least one of the leads; and

e) at least partially encapsulating the leadframe and the semiconductor chip with an encapsulation material such that at least a portion of the lower lead surface of each of the leads is exposed in the encapsulation material.

13. (New) The method of Claim 12 wherein step (b) comprises etching the leadframe such that each of the leads has a lead thickness between the upper and lower lead surfaces thereof which exceeds a paddle thickness of the die paddle between the top and bottom surfaces thereof.

14. (New) The method of Claim 13 wherein step (b) comprises etching the entirety of the top surface of the die paddle and etching a portion of the lower lead surface of each of the leads in amounts sufficient to cause the lead thickness of each of the leads to exceed the paddle thickness and the top surface of the die paddle to extend in generally co-planar relation to the etched lead surface of each of the leads.

15. (New) The method of Claim 14 wherein the etching of the top surface of the die paddle and the etching of a portion of the lower lead surface of each of the leads to form the half etched portion therein is conducted simultaneously.

16. (New) The method of Claim 12 wherein step (d) comprises electrically connecting the semiconductor chip to the upper lead surface of at least one of the leads via a conductive wire which is encapsulated by the encapsulation material.

17. (New) The method of Claim 12 wherein step (e) comprises applying the encapsulation material such that the bottom surface of the die paddle is exposed therein.

18. (New) The method of Claim 17 wherein step (a) comprises providing a leadframe wherein the bottom surface of the die paddle and the lower lead surface of each of the leads extend in generally co-planar relation to each other.

19. (New) The method of Claim 17 further comprising the step of:

g) plating the bottom surface of the die paddle and the lower lead surface of each of the leads with a corrosion-minimizing material.

20. (New) The method of Claim 12 wherein step (e) comprises applying the encapsulation material such that at least a portion of the upper lead surface of each of the leads is exposed therein.

21. (New) The method of Claim 12 wherein step (a) further comprises plating the upper lead surface of at least one of the leads with an electrical conductivity enhancing material.

22. (New) A method of fabricating a leadframe for use in a semiconductor package, comprising the steps of:

a) providing a die paddle having opposed, generally planar top and bottom surfaces, and a plurality of leads which extend at least partially about the die paddle and each have opposed, generally planar upper and lower lead surfaces and an inner end; and

b) etching the die paddle and the leads such that each of the leads includes a half etched portion which is formed in the lower lead surface, extends to the inner lead end, and defines a generally planar etched lead surface which is disposed in opposed relation to the upper lead surface and extends in generally co-planar relation to the top surface of the die paddle.

23. (New) The method of Claim 22 wherein step (b) comprises etching the die paddle and the leads such that each of the leads has a lead thickness between the upper and lower lead surfaces thereof which exceeds a paddle thickness of the die paddle between the top and bottom surfaces thereof.

24. (New) The method of Claim 23 wherein step (b) comprises etching the entirety of the top surface of the die paddle and etching a portion of the lower lead surface of each of the leads in amounts sufficient to cause the lead thickness of each of the leads to exceed the paddle thickness and the top surface of the die paddle to extend in generally co-planar relation to the etched lead surface of each of the leads.

25. (New) The method of Claim 24 wherein the etching of the top surface of the die paddle and the etching of a portion of the lower lead surface of each of the leads to form the half etched portion therein is conducted simultaneously.

26. (New) The method of Claim 22 further comprising the step of:

c) plating the bottom surface of the die paddle and the lower lead surface of each of the leads with a corrosion-minimizing material.

27. (New) The method of Claim 22 further comprising the step of:

g) plating the upper lead surface of at least one of the leads with an electrical conductivity enhancing material.

28. (New) A semiconductor package, comprising:

a leadframe comprising:

a die paddle defining opposed, generally planar top and bottom surfaces;

at least one tie bar attached to and extending from the die paddle; and

a plurality of leads extending at least partially about the die paddle in spaced relation thereto, each of the leads having:

opposed, generally planar upper and lower lead surfaces; and

a half-etched portion formed within the lower lead surface, the half-etched portion defining an etched lead surface which is disposed in opposed relation to the upper lead surface;

a semiconductor chip attached to the top surface of the die paddle and electrically connected to at least one of the leads; and

an encapsulation material at least partially encapsulating the leadframe and the semiconductor chip such that at least the lower surfaces of the leads are exposed in the encapsulation material;

the leadframe being formed in the manner wherein the tie bar is sized and configured to interlock the die paddle to the encapsulation material.

29. (New) The semiconductor package of Claim 28 wherein the tie bar includes:

opposed, generally planar upper and lower tie bar surfaces; and

a half-etched portion formed in the lower tie bar surface and defining an etched tie bar surface which is disposed in opposed relation to the upper tie bar surface;

the etched tie bar surface being covered with the encapsulation material.

30. (New) The semiconductor package of Claim 29 wherein the lower tie bar surface is exposed in the encapsulation material and extends in generally co-planar relation to the lower lead surfaces of the leads.

31. (New) The semiconductor package of Claim 29 wherein the etched tie bar surface extends in generally co-planar relation to the etched lead surface of each of the leads.